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International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 : H04N 5/445, 7/08 — A1

(11) International Publication Number: WO 85/ 02082

(43) International Publication Date: 9 May 1985 (09.05.85)

(21) International Application Number: PCT/GB84/00363

(22) International Filing Date: 26 October 1984 (26.10.84)

(31) Priority Application Number: 8328601

(32) Priority Date: 26 October 1983 (26.10.83)

(33) Priority Country: GB

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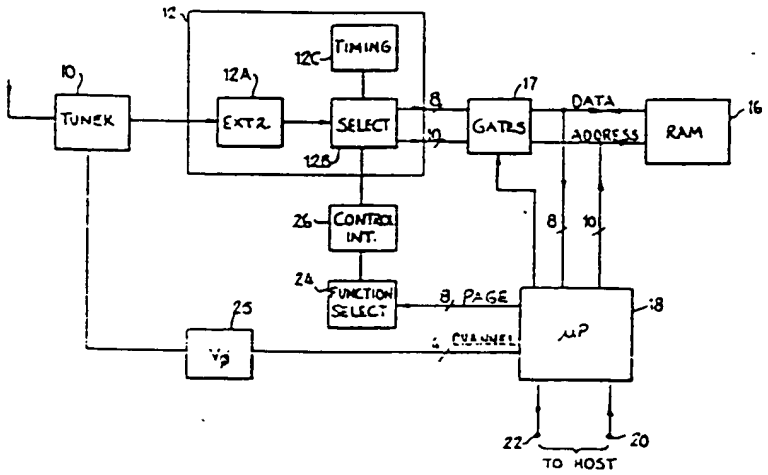
(81) Designated States: AT (European patent), AU, BE (European patent), CH (European patent), DE, DE (European patent), FR (European patent), JP, KR, LU (European patent), MC, NL (European patent), SE (European patent), US.

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: DATA RETRIEVAL SYSTEM



(57) Abstract

A data retrieval system, intended principally for allowing a computer to make use of the viewdata or teletext information services, stores selected portions of data corresponding, for example, to one of the pages of transmitted information and feeds the data one byte at a time to the computer in the order in which alphanumeric characters represented by the bytes appear on the page. To do this, data selected in real time by a teletext or viewdata decoder (12) is written to a random access memory (16) during a predetermined time interval sufficient to accumulate a page of information in the memory, and stored in the memory (16) in an interlaced line format. After the time interval, a microprocessor (18), with the aid of a look-up table, reads out the lines of data from the memory one byte at a time in the order that the lines appear in the page, and converts these bytes to a serial ASCII coded data stream suitable for storage, processing or display in a number of different types of host computer. The system also allows commands, such as page numbers, to be converted to a form suitable for controlling the selection of data in the decoder (12).

DATA RETRIEVAL SYSTEM

This invention relates to a data retrieval system using information services such as teletext and viewdata whereby information is broadcast or is available through television and telephone networks in the form of pages of information comprising generally lines of text and figures.

For some years broadcasting organisations in the United Kingdom have provided teletext information services whereby a domestic television receiver equipped with a suitable decoder can be used to display written and pictorial information broadcast as a composite video signal comprising a digital signal interleaved with the standard analogue picture signal. The digital signal comprises a string of 8-bit symbol codes (bytes) transmitted serially together with synchronisation bytes. The decoder contains timing circuits to extract the digital signal from the received composite video signal and then write the 8-bit bytes one after the other in parallel form to a random access memory (RAM) where they are stored until a complete page of information has been written in. At this point, the data is fed at a relatively high rate to a character generator so that the page of information can be displayed on the TV screen. The teletext decoder provides control and select functions whereby, for example, commands from a handheld infra-red transmitter module are used to control data acquisition from the incoming serial signal so that only data corresponding to a required page of information is stored in the RAM prior to displaying it. Due to the effective bandwidth limitations imposed by the use of a composite video signal, acquisition of a complete page of information can take up to 24 seconds.

A similar system, known as 'viewdata' has been developed for transmitting data in a corresponding format using a conventional telephone line. Again, a domestic television receiver, in this case connected to telephone subscriber apparatus with a suitable adaptor, is used to display the information. The viewdata system

does not suffer from the same response time disadvantage as the teletext system, but has in common with the teletext system the disadvantage that information cannot be used to full potential. In other words, it can only be displayed in transient form, or stored for example on magnetic tape for later display, provided suitable tape recording apparatus compatible with the viewdata decoder is available.

This invention increases the versatility of teletext and viewdata systems by converting the received data to a form whereby it can be processed by computer equipment. The invention provides a method of retrieving data from a data signal transmitted over a public transmission medium in the form of a serial data stream having a series of coded pulse groups corresponding to alphanumeric characters arranged in lines and in pages each having a plurality of lines, the method comprising the steps of: (i) receiving the signal from the medium; (ii) selecting portions of the signal corresponding to a required page, said selection taking place in real time; (iii) writing the selected portions in real time to a memory as they are received and selected, the addressing of the memory being arranged so that bytes representing the alphanumeric characters are stored in a predetermined format; (iv) reading the stored bytes from the memory to a data processor in an order corresponding to the order of the characters in the lines and in the order of the lines in the page; (v) receiving page selection commands; (vi) from the commands, generating command signals having a predetermined format for controlling the selection of said data portions as they are received. In this way, data received from the transmission medium is put into a format for output using an industry data transmission standard such as the RS232 standard, so that the interface unit can transmit data to and receive commands from a host computer. Using the invention data transmitted by teletext or viewdata services can not only be displayed at a computer location remote from the interface unit, but it can also be manipulated and stored in ASCII format by the host computer to act as a part of a useful database. A typical application for the invention is in organisations where foreign currency transactions depend

on accurate knowledge of exchange rates. The teletext and viewdata services broadcast exchange rate data which is regularly and frequently updated. Apparatus used in accordance with this invention enables the exchange rates to be monitored and stored by manually or automatically selecting the relevant 'page' of information and extracting the required characters for entry into the database. The host computer then has an up-to-date list of exchange rates which may be reported and used within the database in a manner determined by the user.

According to a second aspect of the invention the method described above may be performed using a circuit arrangement for interfacing a teletext or viewdata decoder with a computer, the decoder having a selector device for selecting required portions of a received data stream corresponding to a selected page of alphanumeric characters in accordance with command signals applied to a control input, the arrangement comprising a memory coupled to the selector device for receiving and storing the selected data portions in a predetermined format, a data processor programmed to read data out of the memory in an order corresponding to the order of the characters in the page and to transmit the data to the computer in a form compatible with the computer.

The invention will now be described by way of example with reference to the drawings in which:-

Figure 1 is a block diagram of a data retrieval system in accordance with the invention for receiving data from a teletext service;

Figure 2 is a diagram illustrating the arrangement of bytes of a page of teletext information when stored in a teletext decoder module prior to processing;

Figures 3A - 3D are a circuit diagram of part of the system of Figure 1;

Figure 3 is a diagram showing how Figures 3A - 3D are put together;

Figure 4 is a simplified flow chart illustrating the operating sequence of the system of Figures 3A - 3D;

Figure 5 is a flow chart showing how the system is initialised;

Figure 6 is a flow chart showing how the memory of the system is updated with teletext data;

Figure 7 is a flow chart illustrating the operations needed to send a character to the host computer or to receive a character therefrom;

Figures 8A and 8B, when laid side by side, are a flow chart illustrating how the system processes a command received from the host computer; and

Figures 9A and 9B, when laid side by side, are a flow chart showing the operations necessary for reading out a page of data from the memory and sending it to the host computer.

Referring to Figure 1, a system for retrieving teletext data and converting it into a form suitable for use by a host computer has firstly a UHF tuner 10 and teletext decoder 12 which may be part of a conventional teletext decoder module such as that manufactured by Mullard Limited under the type number VM6101. The decoder 12 receives a composite video signal from the tuner 10 and, in a first stage 12A, extracts the teletext serial data signal. According to command signals present on a control input 14 of the decoder 12, data corresponding to a particular page of teletext information is selected from the serial data signal by a second stage 12B under the control of a third, timing stage 12C, and fed word by word to a random access memory (RAM) 16.

In a teletext decoder for displaying teletext data directly on a television screen in a known manner, the data is stored temporarily in a RAM in a format determined by the manner in which the television screen is scanned, so that each displayed character is built up on the screen as a series of dots which are produced by signals fed from the RAM in an order different from the order of the characters in each line. In the present system the RAM 16 is filled in a different format so that within each line the characters or bytes are in an order corresponding to the order in which they are positioned in the displayed line. The required order of characters within each line is determined by the scheme of interconnection of the decoder address lines to the RAM address inputs as will be described hereinafter. The result of the addressing scheme is that the data is stored in an interlaced line format as shown in Figure 2. Each line of information is 40 characters long, each box in Figure 2 representing 8 bytes of data. The RAM locations are filled in the interlaced line format in accordance with the sequence of address line connections between the RAM 16 and integrated circuits in the module 12, the filling of RAM locations continuing in the pattern shown until the RAM 16 is full and a complete page of 24 lines has been stored.

The tuner 10 and teletext decoder 12 are thus used in a similar manner to that in which they are used in a conventional teletext equipped television set for receiving teletext services. However, rather than using the stored page data to generate characters on a television screen, the present system provides an interface including a microprocessor circuit 18 which controls the RAM 16 to store a complete page of data and re-orders and converts the data into a form which can be processed by a variety of different types of computer systems, ranging from personal computers to mainframe computers. Operation of the mircroprocessor circuit 18 is controlled by a program responsive to commands received via a serial input port 20 from a remote host computer (not shown). Typically this port is RS232 compatible. The program enables the microprocessor circuit 18 to read out the stored teletext data from the RAM 16 in the line sequence in which it is to be displayed or stored by the host computer, to convert it into, for example, a serial data stream which is transmitted from an RS232 compatible output port 22. It will be appreciated that once the data has been transmitted to the host computer, selected parts of a page such as exchange rates can be extracted provided their location on the page is known.

The system allows the host computer to control page selection in the teletext decoder 12 and channel selection in the tuner 10. For this purpose the microprocessor circuit 18 is programmed to convert serial ASCII commands received via input port 20 into a parallel format for driving a function select controller 24 and a tuning voltage source 25. Controller 24 drives a control interface 26 which generates an amplitude modulated serial data signal suitable for controlling the selector stage 12B in decoder 12, whilst source 25 produces a tuning voltage for adjusting the operating frequency of the tuner 10.

In the case of teletext, as opposed to viewdata, signals, incoming UHF signals are demodulated in tuner 10, the resulting composite video signal being fed in the teletext decoder 12 to the stages 12A, 12B and 12C which are based on a series of integrated circuits manufactured by Mullard Limited under type

Nos. SAA5030, SAA5040 and SAA5020. None of these i.c.'s are shown in the drawings since they form part of a known decoder module which is a commercially available unit, the manner of their interconnection being described in literature relating to the unit. Data and data clock information is extracted from the composite video signal in the extractor stage 12A (SAA5030) and fed as a serial data stream to the selector stage 12B (SAA5040) which selects data according to a page number set on its control input 14, this data being collected and transmitted as parallel bytes one byte after the other to the RAM 16 (Figure 1) via 8 parallel data lines D0 to D7. The necessary timing signals for the RAM 16 are derived from the timing stage 12C (SAA5020) which maintains synchronisation between the teletext system and the incoming composite video signal. 10 address lines A0 to A9 couple the RAM 16 to address pins on both the SAA5040 and the SAA5020, the order in which the bus lines are connected to the RAM 16 determining the locations in the RAM to which data bytes are written.

Referring now to Figures 3A to 3D, in which the RAM 16 is shown as two 1K RAM chips (type No.2114-L) IC8 and IC9, the data bus D0 to D7 referred to above is coupled via a first connected 30 (Figure 3D) and a multiple TTL transmission gate IC10 (integrated circuit type No.74LS244) to the data pins of the RAM chips in conventional order, with lines D0 to D3 coupled to pins 14 to 11 of RAM chip IC8 and lines D4 to D7 coupled to pins 14 to 11 of RAM 16B. Second and third connectors 36 and 38 couple chip select ($\overline{CS}$), write enable ($\overline{WE}$) and address lines (A0 to A9) from the decoder module 12 (Figure 1) via multiple TTL transmission gates IC6 and IC7 to the address lines of the RAM chips IC8 and IC9, each of which has 10 address lines.

These connections serve for the writing of data bytes from the teletext decoder 12 via the gates IC10, IC6 and IC7 to the RAM chips IC8 and IC9 where a complete page can be stored in interlaced line format as shown in Figure 2. For the reading of the data from the RAM chips to the microprocessor circuit, the data and address lines of the RAM chips and the write enable and chip select lines are also connected to a first input/output port

IC3 (Figure 3C) (type No.8156) coupled to a microprocessor chip IC1. The arrangement of the connections between the teletext decoder 12 on the one hand and the RAM 16 and the I/O port IC3 on the other hand is such that the address pins PAØ to PA7 and PCØ, PC1 correspond respectively to the address lines of the decoder 12 in the following order: A7, A8, A9, AØ, A3, A1, A2, A6, A5, A4.

Referring to Figures 3A and 3C together, the microprocessor chip IC1 (type No.8085), the first I/O port IC3, a second I/O port IC2 (type No.8156), a programmable read only memory (PROM) IC5 (type No.2716/4802), and address line buffer IC4 (type No. 74LS373) all form part of a microcomputer for (i) reading data out of the RAM chips IC8 and IC9 in a predetermined order and transmitting it in serial form to the host computer via line buffer IC17 (type No.1488) and RS232 compatible output port 22, and (ii) receiving serial commands at an input port 20 via a line buffer IC16 (type no.1488) and feeding it to a function select controller (shown as 24 in Figure 1) for channel and page selection by the tuner 10 and teletext decoder 12 respectively. An 8-bit multiplexed data and address bus ADØ to AD7 interconnects the microprocessor IC1 with the two I/O ports IC2 and IC3, and with the PROM IC5 via buffer IC4.

As an alternative, the RS232 compatible ports 20 and 22 shown in Figure 3C may be replaced in a known manner by a USART (Universal Synchronous and Asynchronous Receiver/Transmitter) interface using a device such as the Intel 8251 to allow the use of modem control lines.

The second I/O port IC2 (Figure 3A) couples the microprocessor to a dual-in-line switch array 46 whose settings determine (a) the required baud rate for the transmission and reception of data to and from the host computer, (b) whether the data link is a full duplex or half duplex one, (c) the type of handshake signals, and (d) the data format (depending on the facilities available in the host computer). Port IC2 also serves for the receipt of parallel setting-up bits for the function select controller

comprising two parts. The first part shown in Figure 3A, for channel selection, is a simple buffer IC18 (type No.ULN 2003) for selecting one of four tuning voltages available on four present potentiometers 48A to 48D via relays RR1 to RR4. Four lamps 50 indicate which channel is selected, and an LED bar graph display comprising two LED devices 52A and 52B (both type No.3914) indicates the tuning voltage level. The second part of the function select controller (shown in Figure 3B), for page selection, is a series of gates IC11A, IC11B, IC12A, IC12B, IC13A, and IC13B on three CMOS chips (type No.4529B) which convert the parallel setting-up bits from the port IC2 into a command format suitable for control interface integrated circuits IC14 and IC15 (type Nos.SAA5000A and SAA5012 respectively, manufactured by Mullard Limited) which are interconnected in known manner to provide two control signals for the teletext decoder 12 (Figure 1) at the $\overline{\text{DATA}}$ and DLIM output terminals of IC15. The $\overline{\text{DATA}}$ signal is a 7-bit amplitude modulated digital signal in which groups of data bits designate page numbers, whilst the DLIM signal is a clock signal used by the decoder 12 as a reference for receiving the $\overline{\text{DATA}}$ signal. The overall function of the mircoprocessor, function select controller, and control interface with regard to the control of the decoder 12 is to convert serial ASCII commands, e.g. page "158" into the 7-bit serial $\overline{\text{DATA}}$ signal compatible with the decoder 12, specifically with the control inputs of the SAA 5040 integrated circuit in the decoder 12, as referred to earlier in this description.

The PROM IC5 (Figure 3C) stores mainly the operating software for the microprocessor IC1, a look-up table governing the setting-up bits corresponding to ASCII command signals received from the host computer, and a look-up table determining the order in which data lines are read out of the RAM. The operation of the mirco-processor as governed by the software will be described below with reference to the flow charts of Figures 4 to 93, but first it is convenient to summarise the operation of the system as a whole with reference to Figures 1 and 3A to 3D.

Broadcast television signals are received in tuner 10 and the demodulated composite video signal is fed to the teletext decoder 12 where the teletext data is extracted. The extracted

data is supplied in serial form in the decoder to the SAA5050 selector stage 12B in the decoder, which, according to the control signals fed to its $\overline{\text{DATA}}$ input 14 from the control interface 26, selects particular pages of the incoming teletext data from the incoming stream and writes the selected data in real time byte by byte into the RAM 18 (IC8 and IC9 in Figure 3D) in an order governed by the address line connections between the RAM and the selector stage 12B. (In the case of viewdata signals received over a telephone line, the tuner 10 and demodulator part 12A of the decoder 12 are largely dispensed with, the signals being fed directly via a telephone line interface to a selector stage.)

The RAM 16 is controlled by the microprocessor 18 to receive bytes from the selector stage 12B only during specific periods.

When the host computer transmits, for example, a command such as page "158", the microprocessor 18 interprets the command and, with the aid of the look-up table stored in PROM (IC5), it generates plurality of setting-up bits which are in turn converted by the function select controller 24 and the control interface 26 (Figure 1) to the appropriate $\overline{\text{DATA}}$ signals. At the same time as sending the $\overline{\text{DATA}}$ command signals, the RAM 16 is enabled so that over a period of about 12 seconds it stores the teletext data corresponding to the selected pages as it is received from the teletext decoder 12. After 12 seconds the RAM updating is disabled and the stored page of data is read out character by character in the required order, each character being converted preferably to a serial ASCII byte for sending to the computer.

In the case of teletext, channel selection is performed in a similar manner to page selection in that an incoming channel command from the host computer such as "BBC2" is interpreted using the look-up table, and the appropriate setting-up bits transmitted to the channel selection relays RR1 to RR4 (Figure 3A). The appropriate tuning voltage is thus transmitted to varicap tuning diodes in the tuner 10 to tune the tuner to the required TV channel.

Referring now to Figure 4, the basic operating sequence begins at switch on with the initialisation (step 100) of program variables

such as the setting of internal flags and the defining of outputs. In step 101 the ports of the I/O device IC2 and IC3 are set up as inputs or outputs as appropriate and the settings on the dual-in-line switch 46 (Figure 3A) are read, these settings then being examined in steps 102 to 105 to determine whether the host computer handshake type is the ENQ/ACK type or not, whether transmission to the host computer is to be full duplex or half duplex, and whether the host computer data format allows the use of graphics, colour, etc. Step 106 is only necessary if the link between the host computer and the microprocessor is under modem control (USART) as referred to above.

Step 107 enables the microoprocessor interrupts and selects the base channel (in this example BBC1) so that the tuner 10 is set accordingly. This completes the operations performed at switch-on. Thereafter in steps 108 to 114 the processor is waiting for a command, storing the command, processing the command, and transmitting received teletext data to the host computer. All of these steps are elaborated below.

The initialisation procedure shown in detail in Figure 5 is self-explanatory and corresponds to steps 100 to 107 in Figure 4.

Referring to Figure 6, updating of the RAM 16 is one of the operations required in processing a command, which is step 113 in Figure 4. When the processor 18 receives a command the RAM is updated with data from the selected page. Thus, in step 115 the processor reads the status of the ports on IC3 to determine whether the gates IC6, IC7 and IC10 (Figure 3D) are open, and then in steps 116 and 117 it opens the gates if they are not already open. A delay of 12 seconds is allowed by step 118 for updating the RAM from the teletext decoder 12, and then the stored data is sent to the host computer.

The exchange of characters between the microprocessor 18 and the host computer is governed by the flow charts of Figure 7. The input of characters to the microprocessor 18 begins with the processor looking for an input in step 120. If the transmission

link is a duplex link it transmits an echo character back to the host computer (step 121), and if it has received an ENQ handshake signal it transmits an acknowledgement signal ACK (step 122). The end of a command or page number is signified by the characters DC2 and on recognising this the processor processes the command and/or gets the required page from the RAM 16 and sends it to the host computer (step 123). If there is no DC2 end of command terminator or carriage return, the character is either part of a command or a control code, and the processor either respectively stores the command character in the processor buffer or returns immediately to waiting for another character.

The sending of a character to the host computer begins with the disabling of the microprocessor interrupts in step 125, and, in the case of a USART modem controlled system, checks for modem control signals in steps 126 and 127. The character is then sent to the host computer in step 128. After a short delay and the re-enabling of the microprocessor interrupts, and if the system is operating on a duplex link, the processor determines in step 129 whether or not the character it has just sent was an echo of an incoming character from the host computer. If it was, it returns to step 120; if it was not and the character was part of a data string or page from the RAM 16, the processor returns to the routines for processing a command (Figure 8 below) or for sending a page to the host computer (Figure 9 below).

Taking the processing of a command first, and referring to Figure 8, when, for example, the processor has received a DC2 command terminator or carriage return it looks at the buffer (step 130) for a command, and then in steps 131 to 133 determines whether the command is a channel selection command, a reset command, or a toggle flag (i.e. the host computer will not control data transfer). If the command is any of these it either respectively causes the selection of the required channel, initialises the system, or prepares itself to receive further characters from the host computer (step 134). If the command is a page number, none of these tests are satisfied, and the processor checks that the first character is a number (step 135), stores the number, gets the next number, checks it, stores it and so on until it has stored three numbers (all pages must have

three numbers). When it has three numbers (N=3, step 136) it checks that it is within the required range of 99 to 999, opens the gates connecting the RAM 16 to the decoder 12, sets a variable B to 5, and sends each number via the function select controller 24 and interface 26 to the decoder 12, decrementing N from 3 downwards at the same time until N=0 which indicates that all three numbers have been sent (steps 137 to 141). Having sent three numbers to the decoder 12, the processor waits for about 12 seconds to allow the selected page to accumulate in the RAM 16 (step 142), whereupon the RAM is prevented from updating any further (step 143) so that the page can subsequently be read out. In the meantime, the processor checks whether, whilst it was waiting, the host computer tried to interrupt, and, if so, whether the interrupt was a handshake signal ENQ (in which case it sends the acknowledgement signal ACK), or whether it was a 'break' (steps 144 to 147). A 'break' is a command from the host computer requiring that the data in the RAM be sent without waiting for further updating (step 148). If no handshake signal or break signal was received, the identity of the page in the RAM is checked and, if correct, the page is sent to the host computer (steps 149 and 148). The purpose of B is to enable the system to try 5 times if necessary to obtain the required page before transmitting the contents of the RAM to the computer (step 150).

Referring to Figure 9, teletext data is read out of the RAM 16 and sent to the computer as follows. Step 151 clears the host computer input register and sets up a line count B to the number of lines expected (normally 24). Since the teletext data is not transmitted by the TV broadcasting organisations in the order in which it would normally appear on a TV screen, and since the data is first stored in the RAM in a interlaced line format, the mircroprocessor requires a look-up table to determine the order in which data is to be read out of the RAM so that the host computer receives it byte by byte in the correct line order for display. The look-up table, which forms part of the microprocessor program stored in the PROM, is set up in step 152. Next the processor determines from the look-up table which line address

in the RAM is to be accessed first and sets up a column (i.e. byte) count of C=40 (step 153). At this stage the line to the host computer is checked (if the computer has a handshake system) by transmitting the ENQ signal and checking for receipt of the acknowledgement ACK (steps 154 to 157). In step 158 the low and high RAM addresses are set up on the address bus so that the microprocessor can access the RAM, in step 159 the RAM is enabled, and in step 160 the first character is read out of the RAM. In step 161 the RAM is disabled whilst the received character is examined in the following steps. If the host computer has full teletext facilities (colour control codes, etc.) (as indicated by the d.i.l. switch 46 (Figure 3A)), the character is examined to see whether it is a graphics character (step 162) so that the computer can be instructed accordingly by adding an eighth bit to the character (step 163) before converting the character to serial form and sending it to the computer (step 164). If the computer is not indicated by switch 46 as having full teletext facilities the character is examined for being either a normal character, in which case it is sent out to the computer immediately (steps 165 and 164), or a control character, in which case it is examined to see whether it is an alphanumeric character, a graphics control character, or neither of these (steps 166 and 167). An alphanumeric code gives rise to the transmission of a "graphics off" signal to the host computer (step 168) followed by the sending of the character. A graphics control code causes a "graphics on" signal to be fed to the computer (step 169). If it is neither an alphanumeric or a graphics control code, a space is transmitted (step 170).

When the character has been sent, column count C is decremented by 1 and the character read-out processing steps are repeated for the next character, beginning again with the handshake step 154. In this way, a whole line is read out by repeating this loop until C=0 (step 171). Each line is followed by carriage return and the end of line terminator signal DC1 (step 172). If the host computer cannot immediately receive the next line, a wait flag is detected

(see step 133 in Figure 8) and the processor enters the character input routine of Figure 7 (steps 173 and 174) and waits for a 'break' command, handshake signal, or DC2 carriage return signal (steps 175 to 177). When the computer has finished processing the line last sent, it will send the DC2 carriage return signal, the processor decrements the line count by 1 and gets the next line address from the look-up table (153). In this manner the lines of teletext data are read off the RAM in the correct order. (Figure 2 indicates the arrangement of the lines in the RAM.) This continues until the line count B is determined as being zero (step 178), when carriage return and line terminator signals are sent to the host computer and the microprocessor interrupts are enabled (steps 179 and 180). The processor then waits for the next command from the computer.

CLAIMS

1. A method of retrieving data from a data signal transmitted over a data transmission medium in the form of a serial data stream having a series of coded pulse groups corresponding to alphanumeric characters arranged in lines and in pages each having a plurality of lines, the method comprising the steps of:

(i) receiving the signal from the medium;

(ii) selecting portions of the signal corresponding to a required page, said selection taking place in real time;

(iii) writing the selected portions in real time to a memory as they are received and selected, the addressing of the memory being arranged so that bytes representing the alphanumeric characters are stored in a predetermined format;

(iv) reading the stored bytes from the memory to a data processor in an order corresponding to the order of the characters in the lines and in the order of the lines in the page;

(v) receiving page selection commands;

(vi) from the commands, generating command signals having a predetermined format for controlling the selection of said data portions as they are received.

2. A method according to claim 1, wherein the data signal is transmitted in the field blanking interval of a video signal containing picture information, the step of receiving the data signal including extracting it from the video signal.

3. A method according to claim 1, wherein the data signal is transmitted over a public telephone network.

4. A method according to claim 1, wherein the selected data portions are written to the memory via a gate which is controlled to allow updating of the memory only during a predetermined time interval.

5. A method according to claim 1, wherein, for each line of characters, the bytes representing those characters and stored in the memory in locations corresponding to the order of the characters in the line.

6. A method according to claim 5, wherein the data portions are stored in interlaced line format.

7. A method according to claim 5, wherein the selected data portions are written to the memory one byte at a time.

8. A method according to claim 1, wherein the processor is arranged to read the stored bytes out of the memory in parallel format one byte at a time, and to convert each type into a serial group of pulses for transmission to a host computer.

9. A method according to claim 1, wherein the data processor is a microprocessor arranged to transmit the stored data to a host computer as a serial data stream and to receive serial commands from the host computer.

10. A method of data retrieval from a teletext or viewdata data source, the method comprising the steps of:-

(i) receiving a teletext or viewdata data signal from the source;

(ii) selecting portions of data from the received signal as it is being received;

(iii) writing the selected data portions into a memory during a controlled time interval;

(iv) after the time interval, reading the data stored in the memory to a data processor in such a manner that character bytes of the data are read out in a predetermined order;

(v) transmitting the bytes from the processor in the same order in which they are to appear in a required final display of the data;

(vi) generating commands for selecting the said data portions from the received signal; and

(vii) coding the commands to produce command signals for controlling the selection.

11. A method according to claim 10, wherein the processor transmits the bytes to a host computer as a serial data stream.

12. A method according to claim 10, wherein the selected data portions are stored in an interlaced line format and the processor reads the bytes from the memory one byte at a time and in the line order of the final display.

13. A device for interfacing a teletext or viewdata receiver with a computer, the device comprising a memory for storing data received in teletext or viewdata format from a teletext or viewdata decoder in the receiver, a microprocessor programmed to re-order the data contained in the memory and to produce a serial data output signal in which the characters and lines of the data are transmitted sequentially in the order they would normally appear in a teletext or viewdata display produced on a television screen, and means for processing remote serial commands sent to the microprocessor and for transmitting serially command signals to the teletext or viewdata decoder for selecting received data.

14. A circuit arrangement for interfacing a teletext or viewdata decoder with a computer, the decoder having a selector device for selecting required portions of a received data stream corresponding to a selected page of alphanumeric characters in accordance with command signals applied to a control input, the arrangement comprising a memory coupled to the selector device for receiving and storing the selected data portions in a predetermined format, a data processor programmed to read data out of the memory in an order corresponding to the order of the characters in the page and to transmit the data to the computer in a form compatible with the computer.

15. A circuit arrangement according to claim 14, including an address bus coupling the decoder to the memory via a gate device which is responsive to signals from the data processor.

16. A circuit arrangement according to claim 15, wherein the connection arrangement of the address lines of the address bus is such that the selected data portions are stored as a plurality of data bytes, and wherein the order, in terms of memory locations, of the stored bytes representing each line of characters of the page corresponds to the order of the characters in the line.

17. A circuit arrangement according to claim 16, wherein the data processor is programmed to read the stored data line by line from the memory in an order corresponding to the order of the lines in the page.

18. A circuit arrangement according to claim 14, wherein the processor includes a microprocessor.

19. A circuit arrangement according to claim 14, wherein the processor is coupled to a function select controller, the processor and the controller being arranged to convert a serial command received from the computer into a coded parallel format command signal.

20. A circuit arrangement according to claim 19, wherein the function select controller is coupled to a control interface arranged to convert the parallel format command signal into a serial control data stream, and to feed the said control data stream to the control input of the decoder.

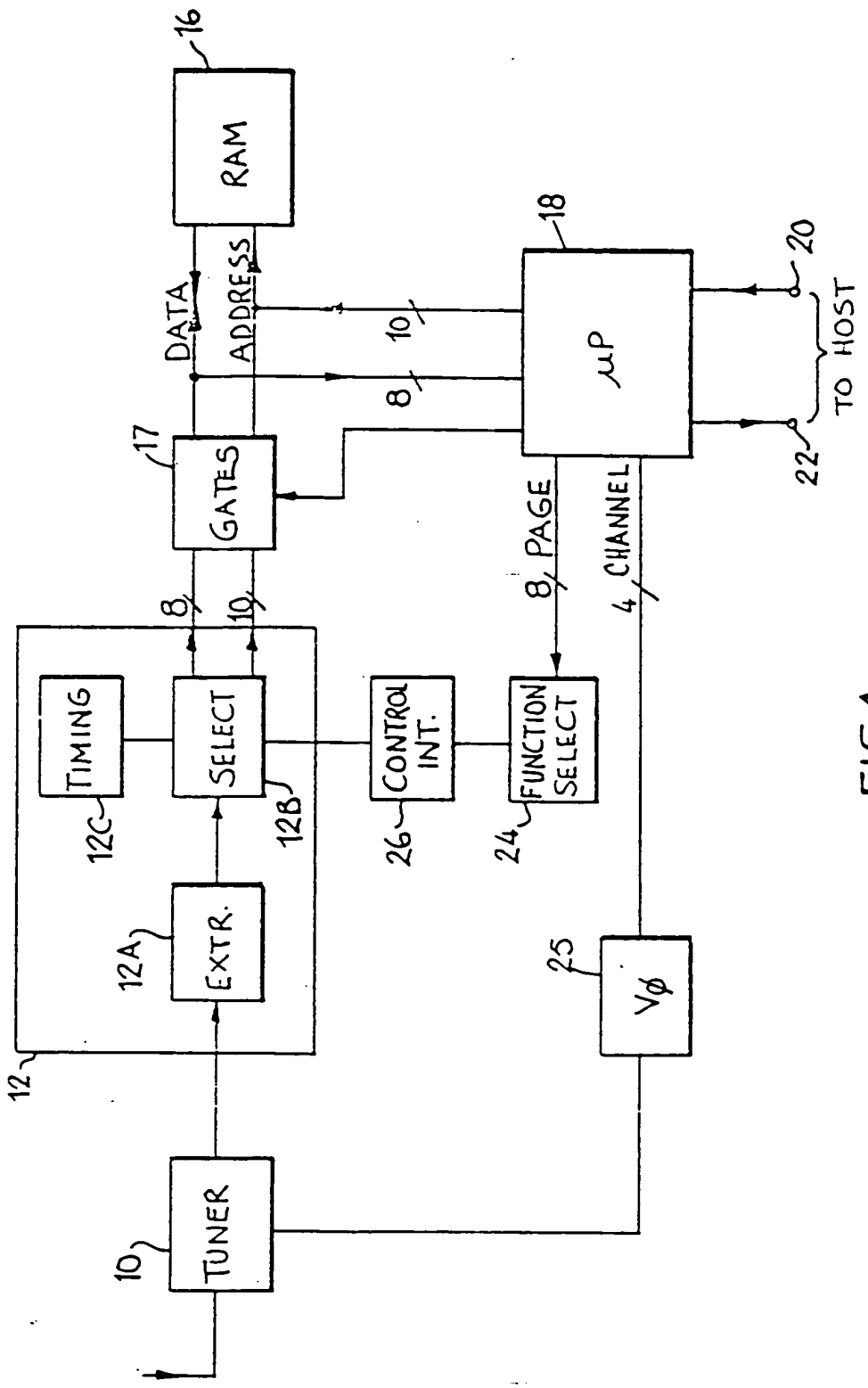


FIG.1.

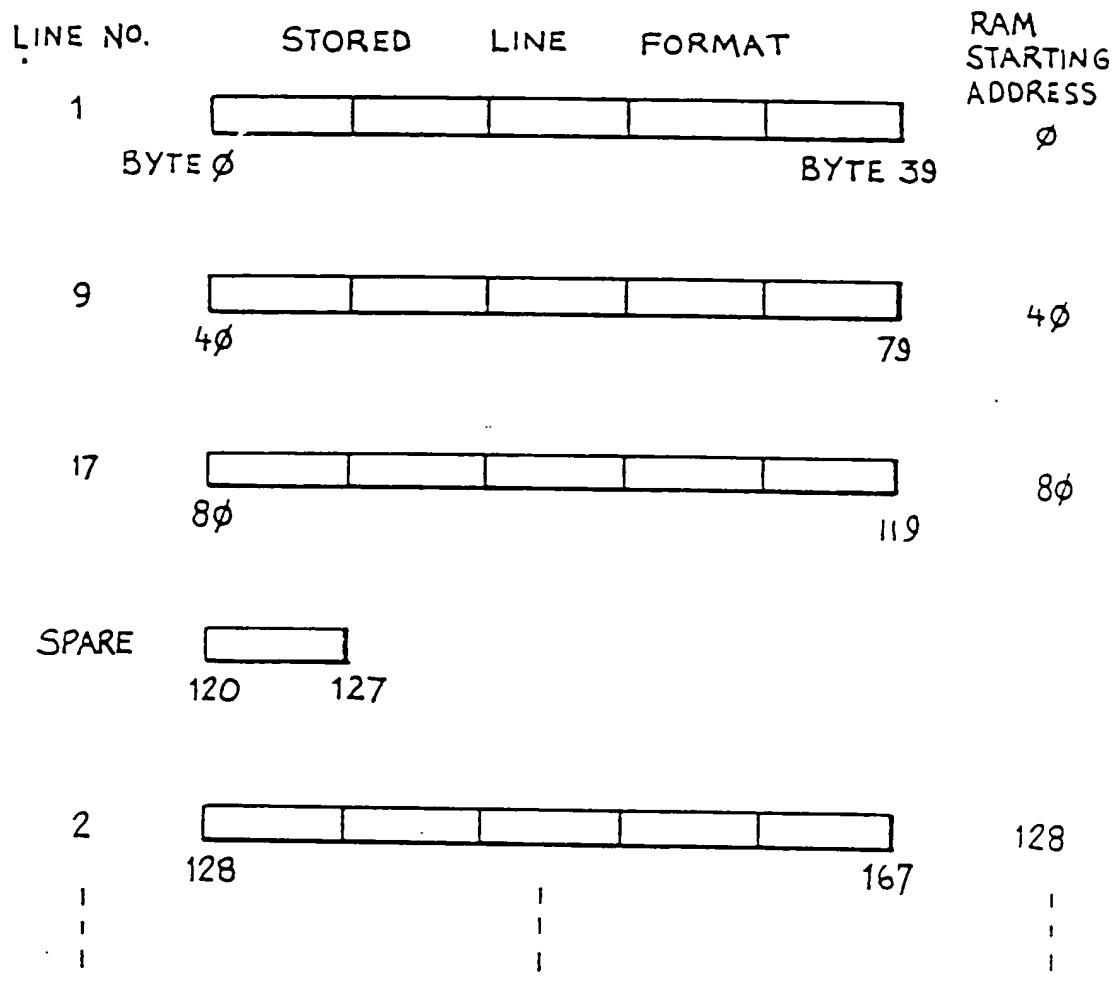


FIG.2.

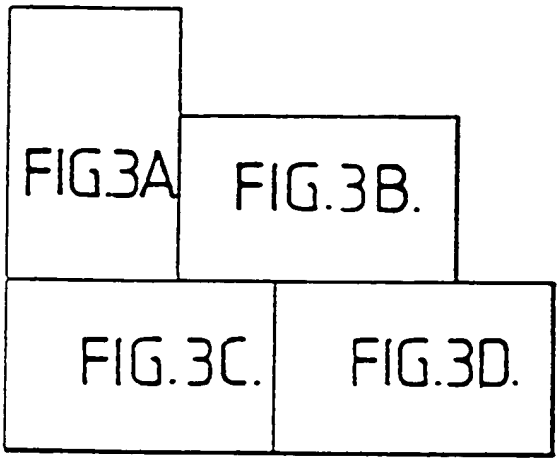


FIG.3.

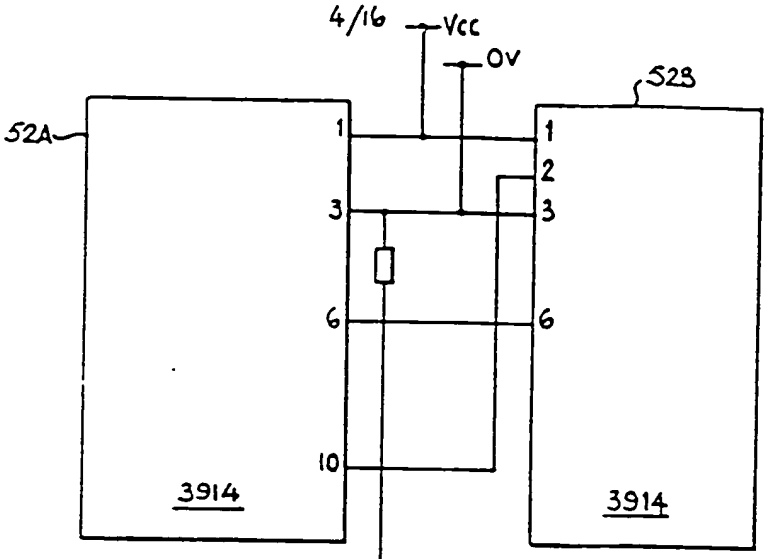
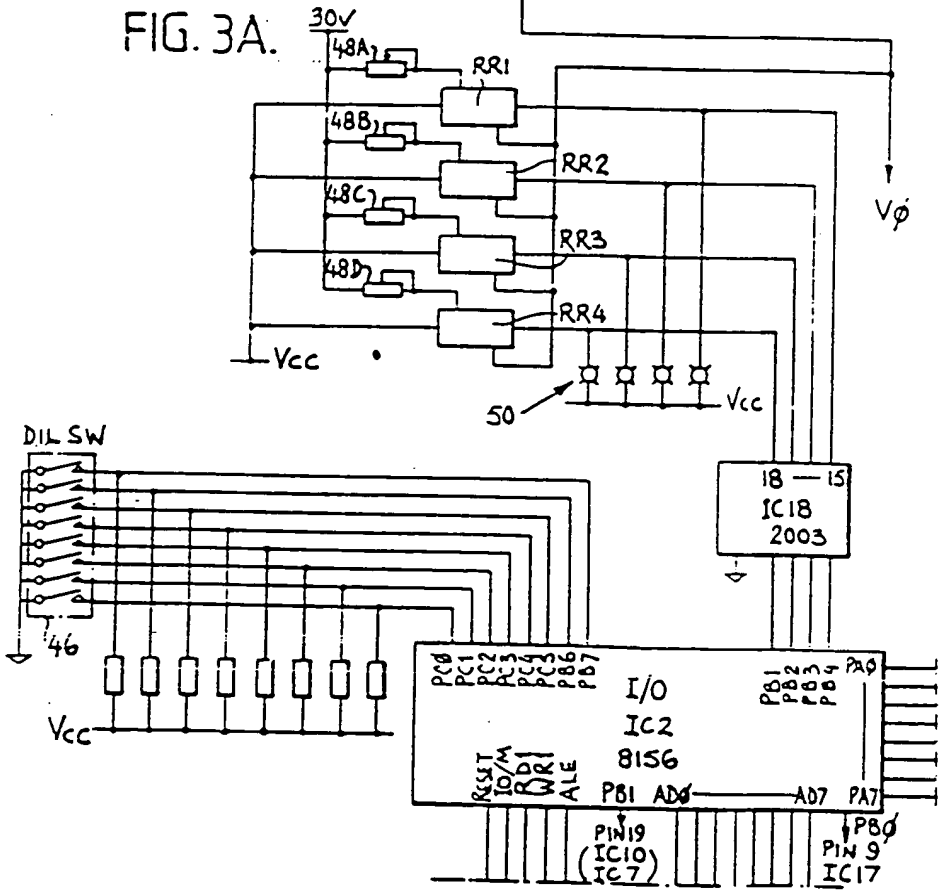


FIG. 3A.



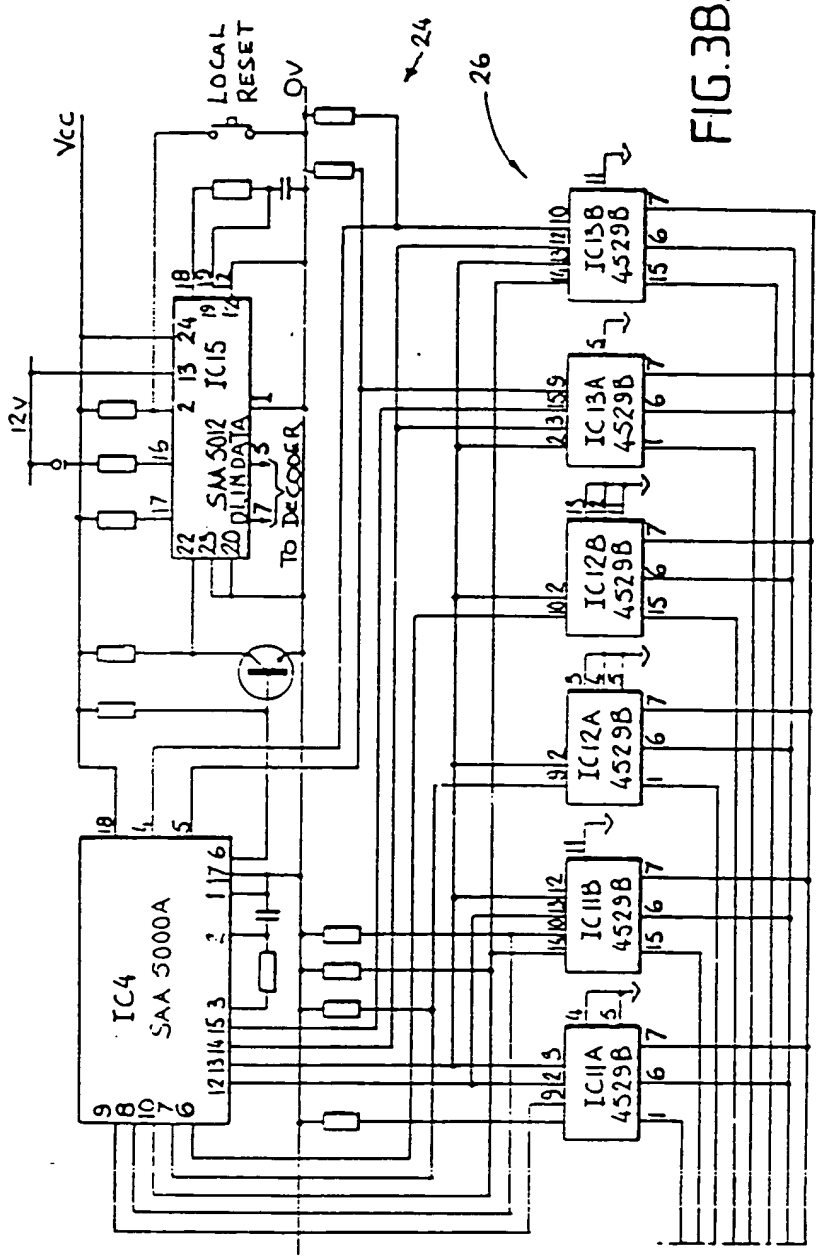


FIG.3B.

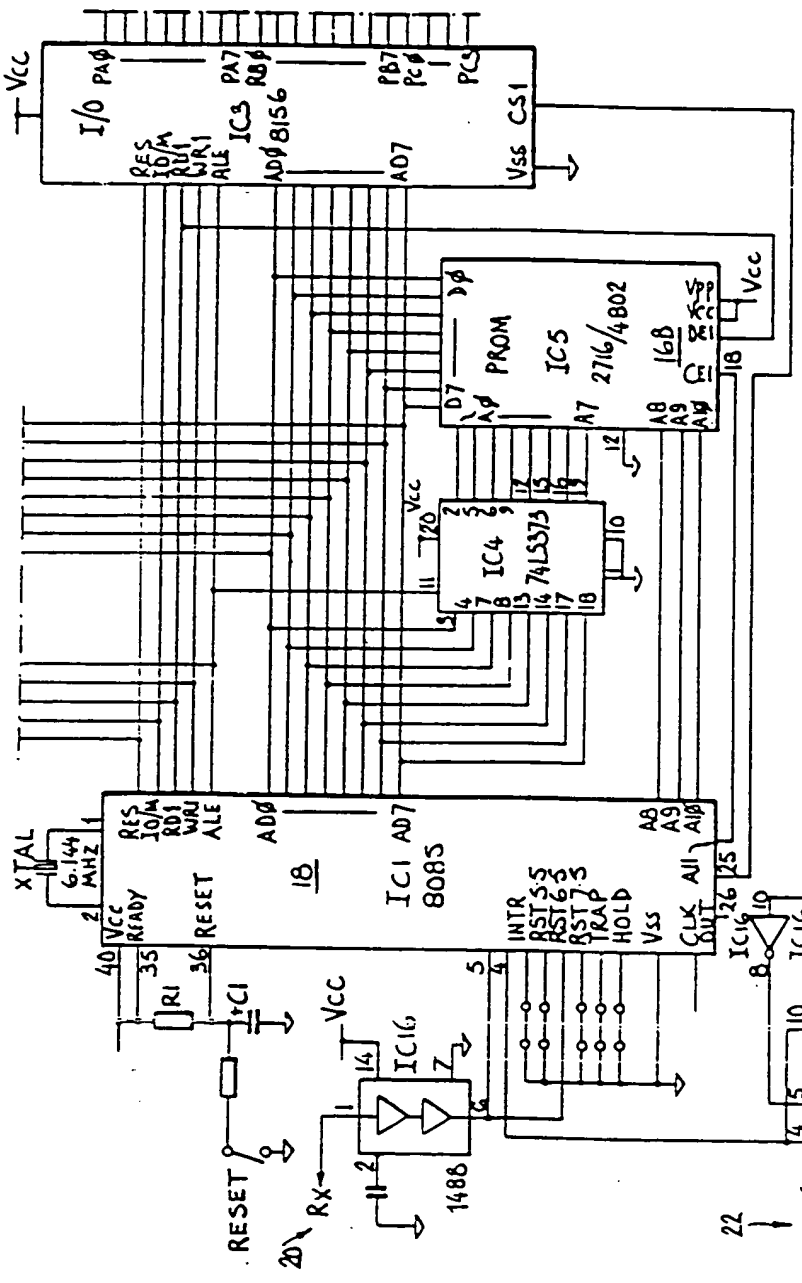
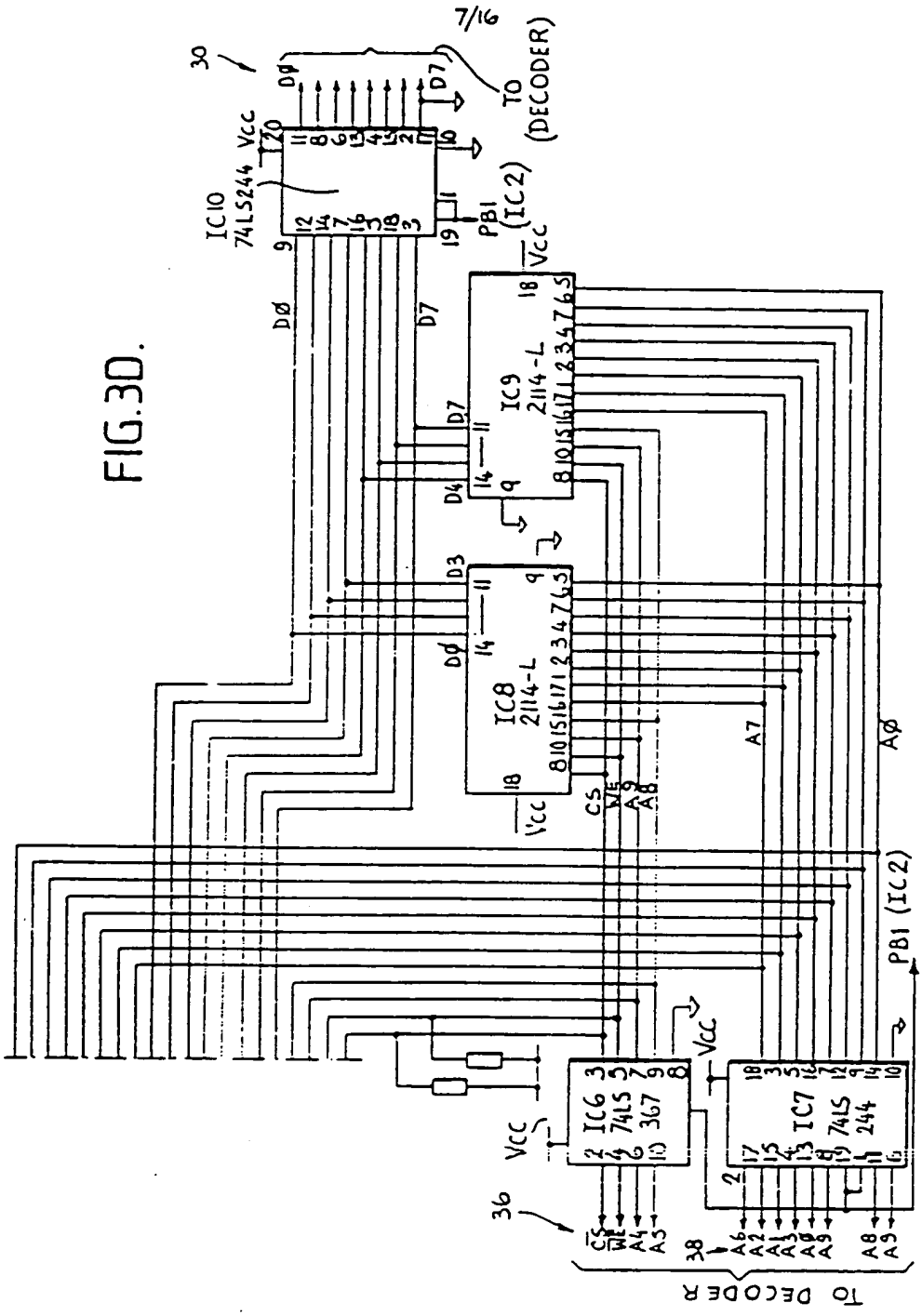


FIG. 3C.

FIG.3D.



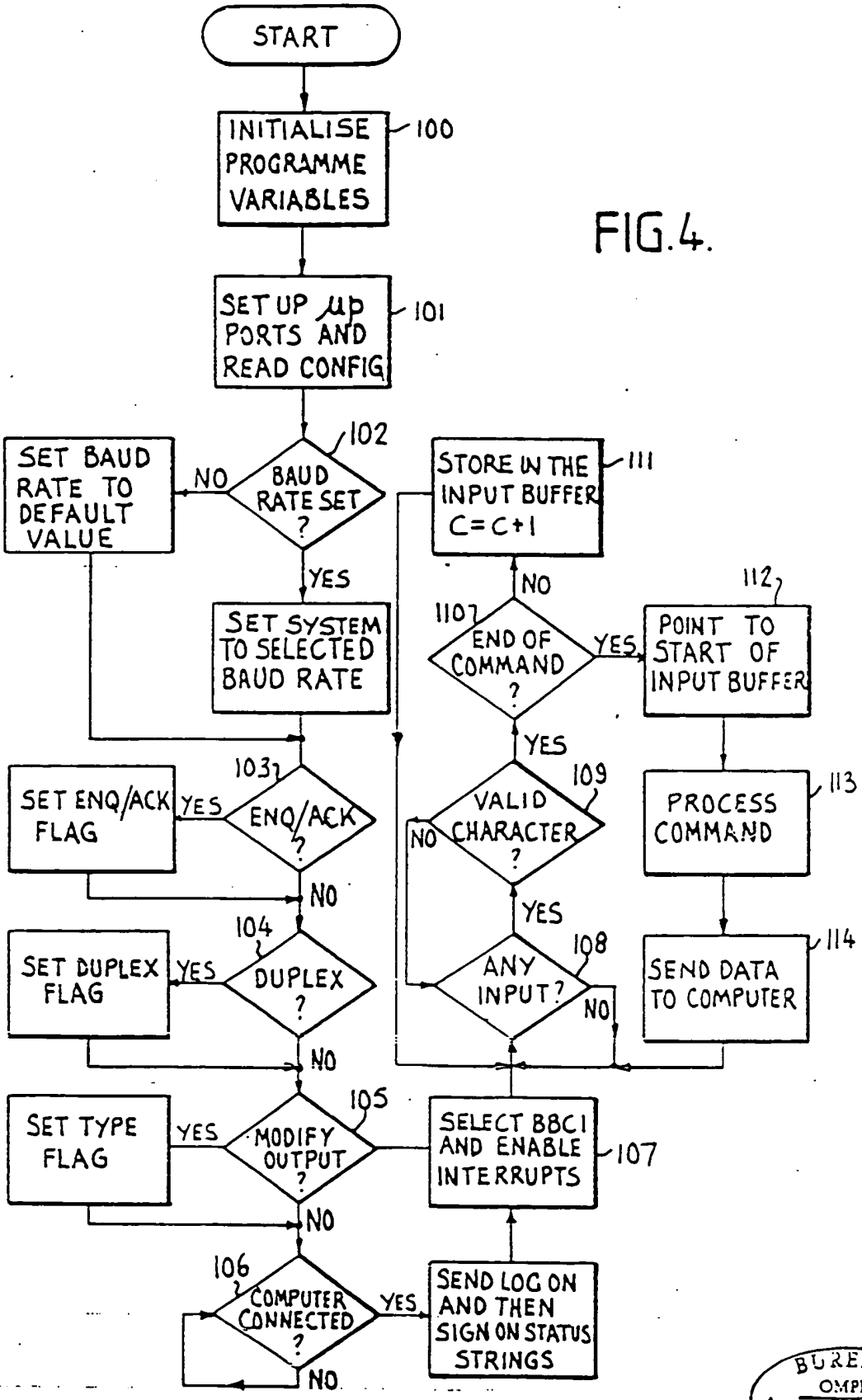


FIG.4.

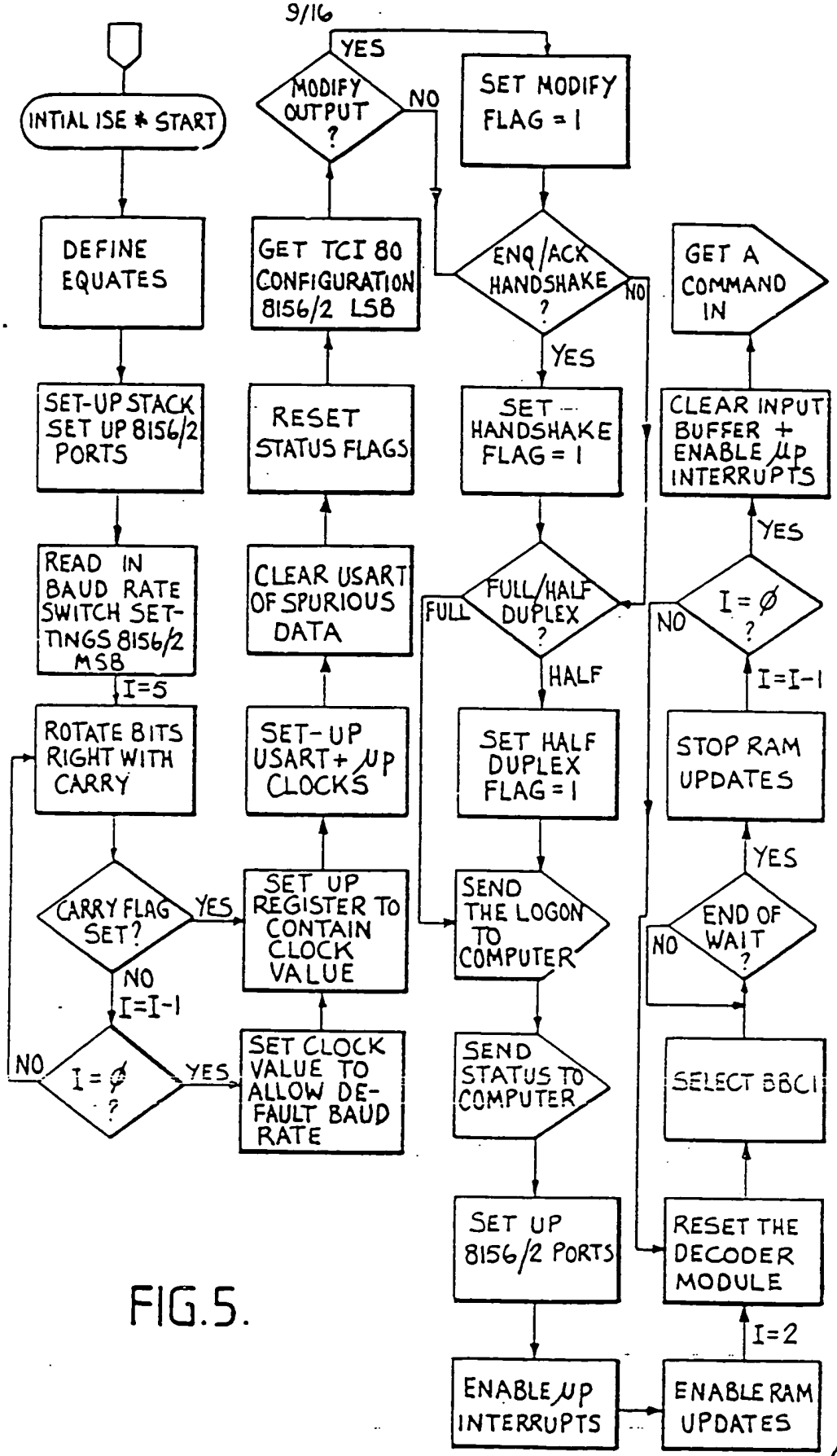


FIG.5.

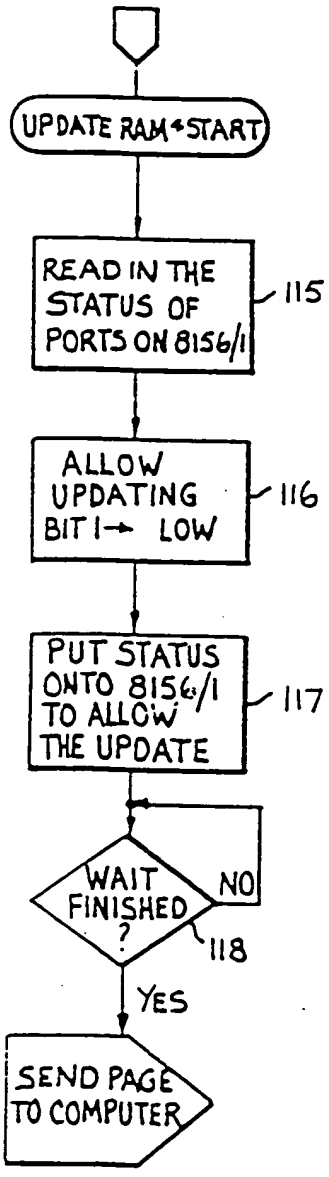


FIG.6.

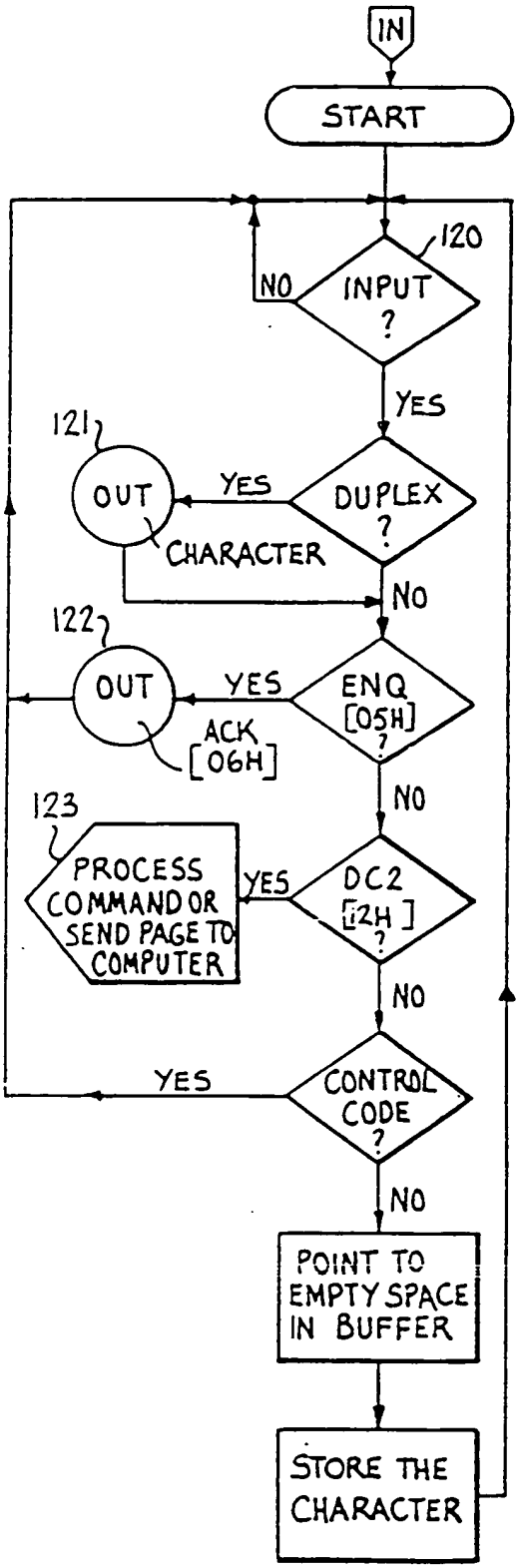


FIG. 7A.

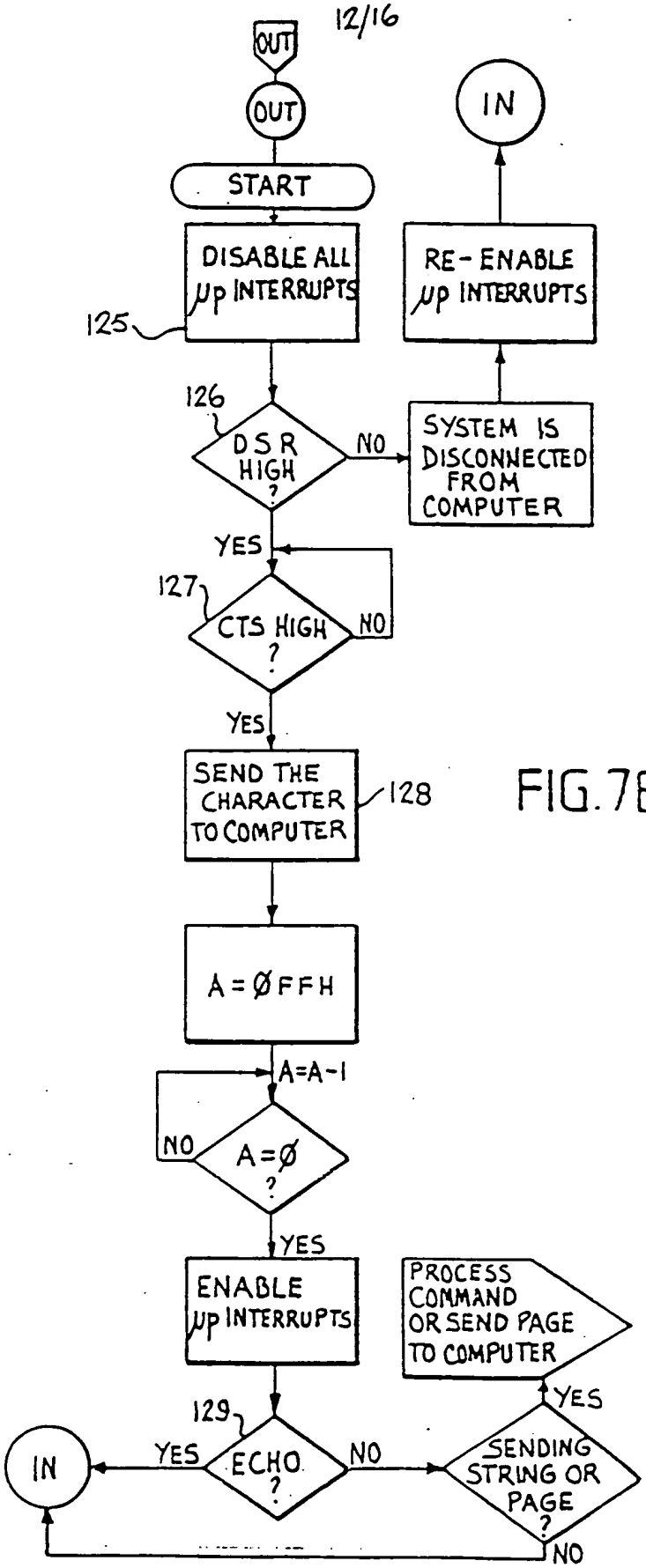


FIG.7B.

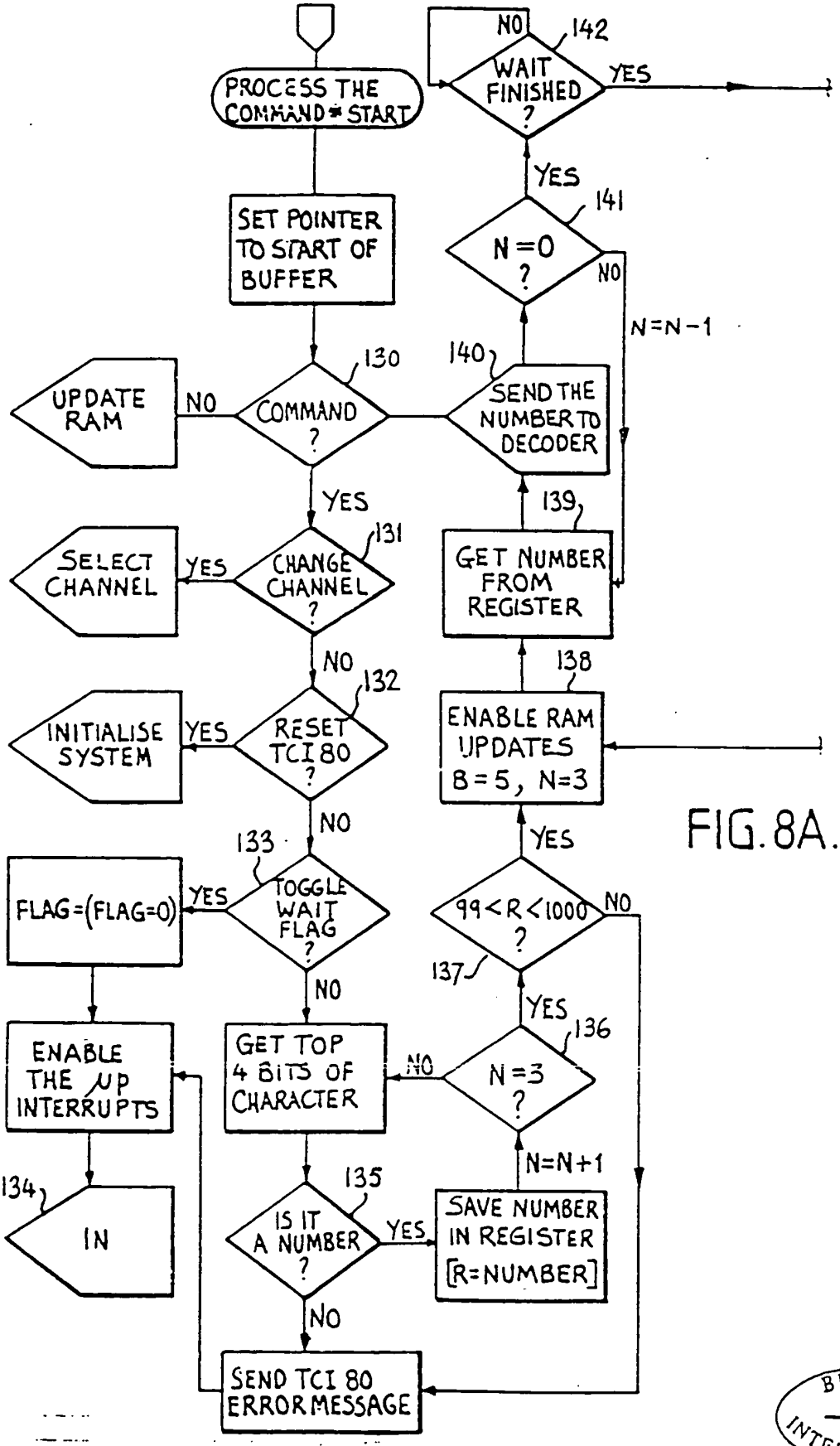


FIG.8A.

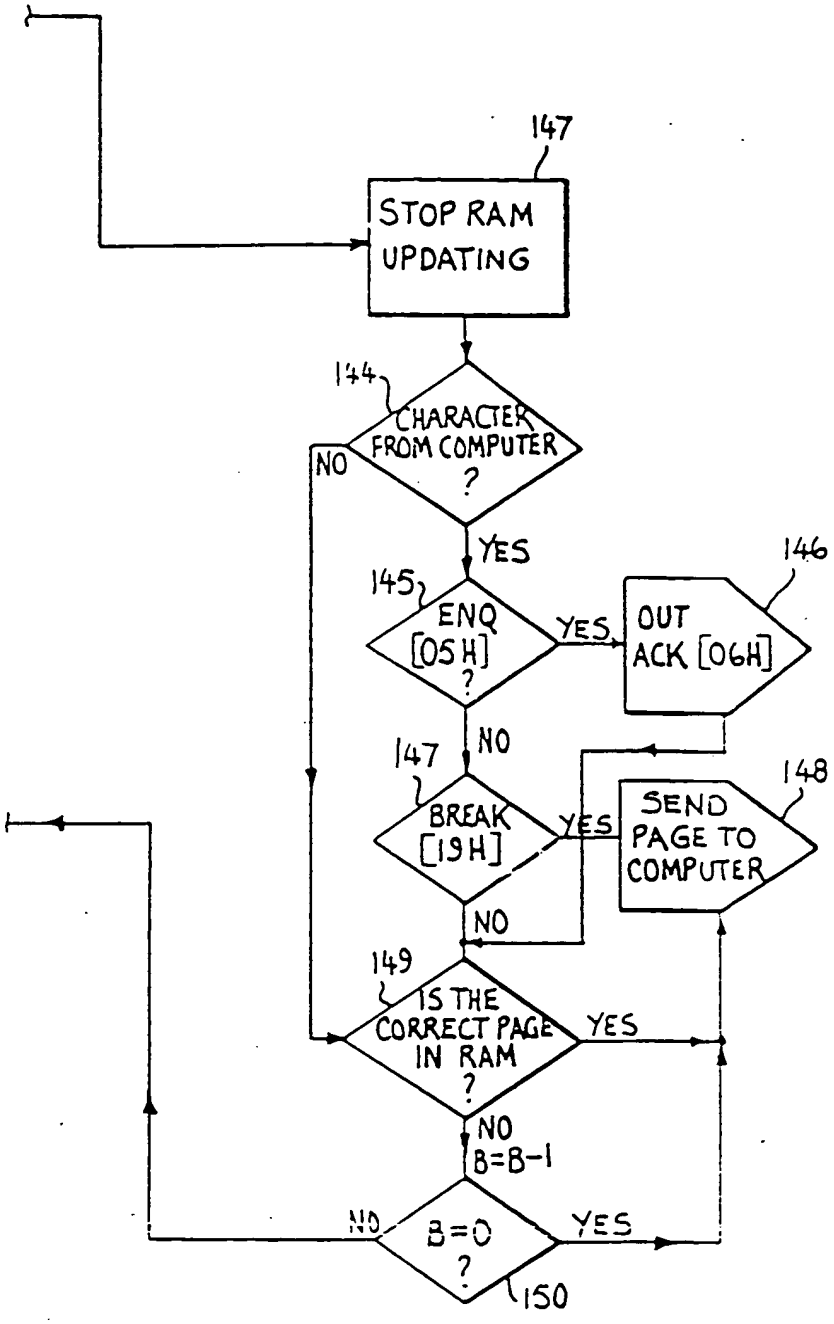


FIG.8B.

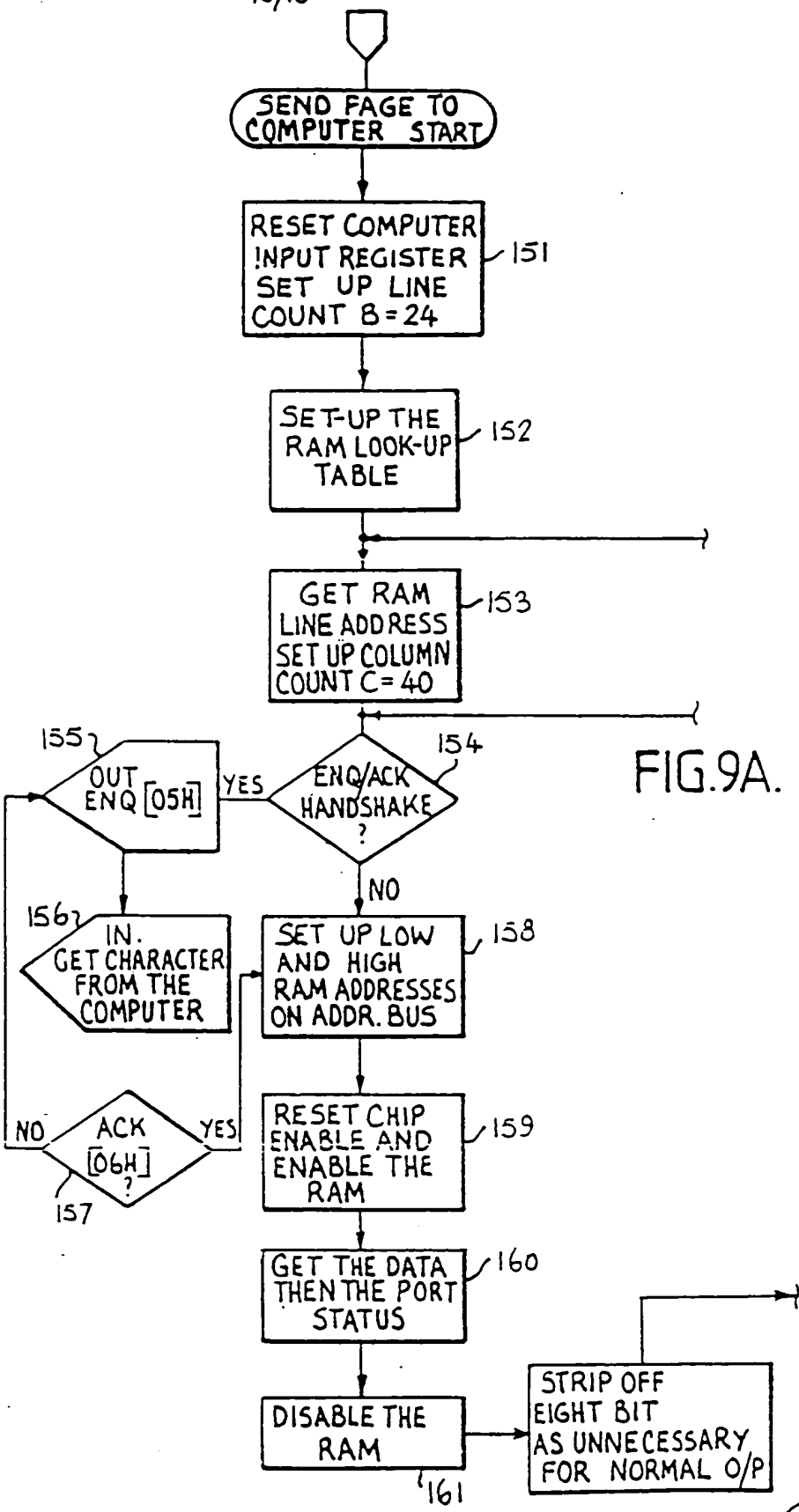


FIG.9A.

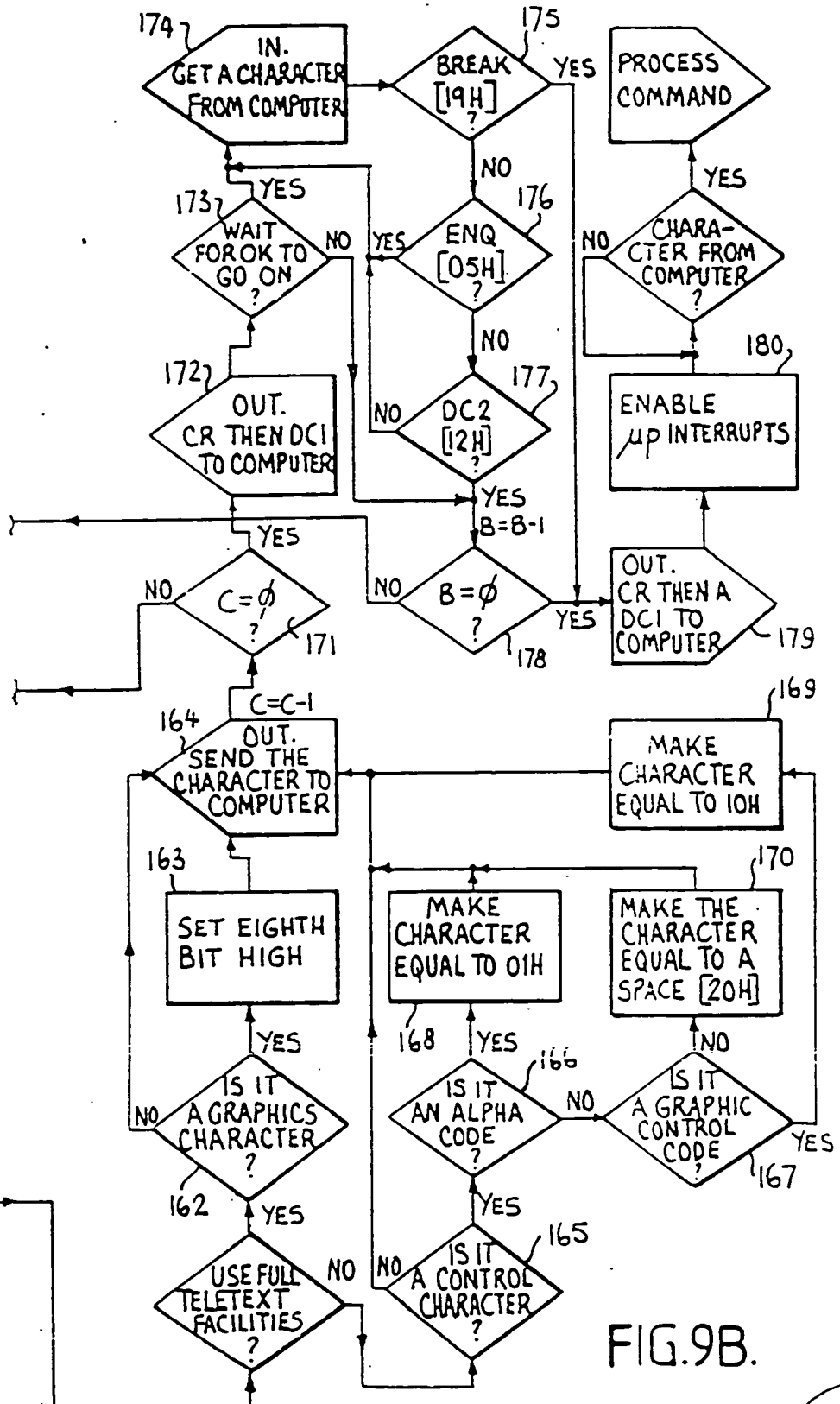


FIG.9B.